DESIGN OF MEDIUM POWER, 6-12 GHz GaAs FET AMPLIFIER, USING HIGH DIELECTRIC NETWORKS

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ABSTRACT

The input and output networks for a 4800μm (four 1200μm cells) gallium arsenide FET amplifier were successfully developed and constructed on high dielectric substrate material using distributed transmission line techniques. This paper describes the design and fabrication of the input and output networks and the performance of a completed 6-12 GHz 4 watt amplifier.

INTRODUCTION

New GaAs FETs for high-power applications at X-band frequencies have been realized by increasing total gate widths at the expense of lowering the devices input impedance and raising the input Q. Obtaining high-power levels over wide bandwidths becomes increasingly difficult as the matching network's combining efficiency decreases due to the high Q FET cells. The use of conventional microstrip matching techniques becomes ineffective as transmission line widths become large and result in dispersion effects. Several successful amplifiers have been built using lumped chip capacitors and bond wires for matching elements, but controlling lengths of wire and capacitance values becomes increasingly difficult and results in degraded performance for wideband high-power applications.[1, 2, 3]

This paper will show a novel approach used in building a 6-12 GHz medium power amplifier using thin high dielectric microstrip circuits for matching the input and presenting a large signal load to the output of the FET cells. Included in the paper will be a description of the measurement and modeling of the 1200μm cell, the design and fabrication of the high dielectric networks, and finally the description and performance of the 6-12 GHz 4 watt amplifier.

MEASUREMENT AND MODELING

The small signal S-parameters of the 1200μm cell were measured on a fixture with 50Ω Quartz transmission lines and connectors which were previously characterized and de-embedded from measurements taken on the automatic network analyzer. S_{11} and S_{22} are shown in Figure 1, and will be used later in designing matching networks. Figure 2 shows a simplified R.F. model of the 1200μm cell without gate-drain capacitance and source inductance. The input matching network is initially designed from the R.F. model and later optimized with the actual measured S-parameter model. The output load network was designed from the R.F. model, but not optimized with the measured S-parameters so the optimum load impedance is not changed.

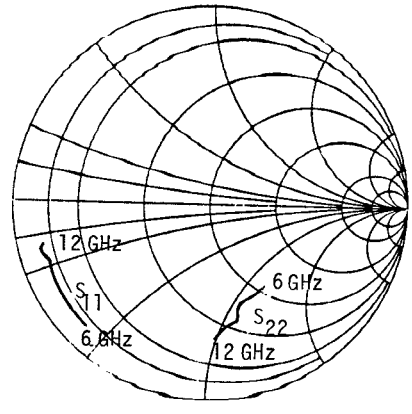

FIGURE 1. MEASURED S_{11} AND S_{22} OF 1200μm FET.

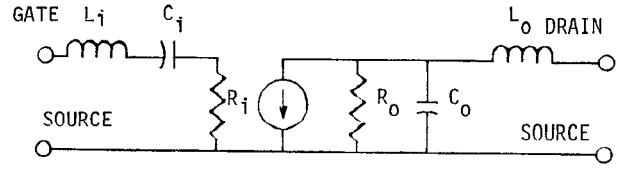

FIGURE 2. RF MODEL OF 1200μm FET. L_i = .09nH, C_i = 1.6pF, R_i = 150Ω, C_o = .33pF, L_o = .09pF.

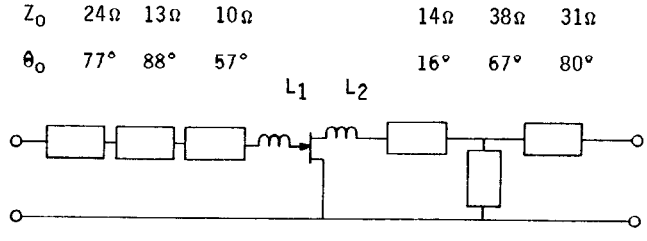

FIGURE 3. MATCHING NETWORK FOR 1200μm FET. Z AND θ ARE TRANSMISSION LINE IMPEDANCE AND ELECTRICAL LENGTH AT 10 GHz, L_1 = .09nH, L_2 = .56nH

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CIRCUIT DEVELOPMENT

The 4800μm FET from Texas Instruments was chosen for its gain and large-signal capabilities at X-band. To realize the 4800μm FET gate width four 1200μm cells are placed in parallel, each cell measuring .508 x .559mm in size. The microwave input signal must be divided, fed to each cell, and then recombined. In order to efficiently divide and recombine the signal, the parallel matching networks must have the same electrical lengths to avoid signal cancellation.

Maximization of large-signal output power also requires the output of the FET to have an optimum load impedance which is different from that required for a small-signal match.[4] Equalization techniques must then be used to compensate for gain deviation which results when the FET is operated into the large-signal load.

The optimum load impedance is calculated from the available current and voltage swing of the FET under large signal conditions. The 1200μm cell was found to require an optimum load of approximately 37Ω with the FET parasitics, C_o, absorbed in the output network. The output network shown in Figure 3 was designed from the R.F. model by setting R_o from 150Ω to 37Ω. The first two series elements and the shunt stub are designed to absorb the parasitics of C_o and the last series transmission line transforms the 37Ω load to the 50Ω system.

The input of the FET presents a much different problem, in that a very low impedance transformer is needed to transform the 3.5Ω of each parallel cell to the 50Ω system over the octave bandwidth. The R.F. model is used to initially design the input network, which is later optimized with the measured S-parameters and output load for optimum gain. The resulting input matching network shown in Figure 3 is not realizable with conventional distributed matching techniques because of the low impedance and small size of the 4800μm FET.

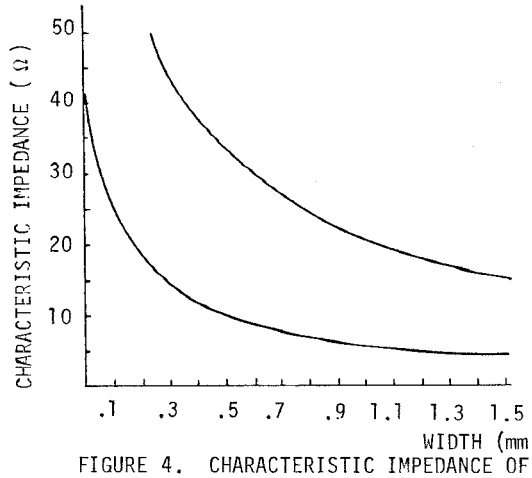

FIGURE 4. CHARACTERISTIC IMPEDANCE OF ALUMINA AND HIGH DIELECTRIC MATERIAL (Kr=64)

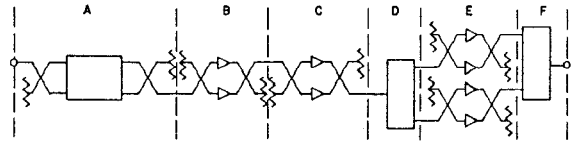

FIGURE 5. AMPLIFIER CHAIN.
A. BALANCED EQUALIZER
B. BALANCED 2400μm FET AMPLIFIER
C. BALANCED 4800μm FET AMPLIFIER
D,F. WILLKINSON POWER DIVIDER (SEE FIG.7)
E. DUAL BALANCED 4800μm FET AMPLIFIER.

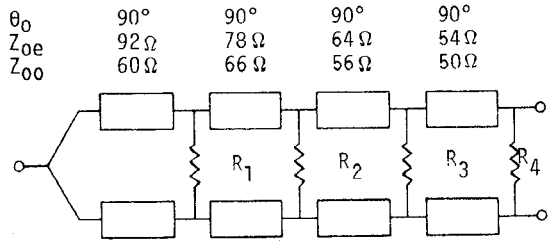

FIGURE 7. FOUR SECTION WILKINSON POWER DIVIDER. ISOLATION RESISTORS ARE; R_1 = 87Ω, R_2 = 142Ω, R_3 = 269Ω, R_4 = 613Ω; COUPLED TRANSMISSION LINE IMPEDANCES ARE Z_{oe} AND Z_{oo}, AND θ_o IS ELECTRICAL LENGTH AT 10 GHz.

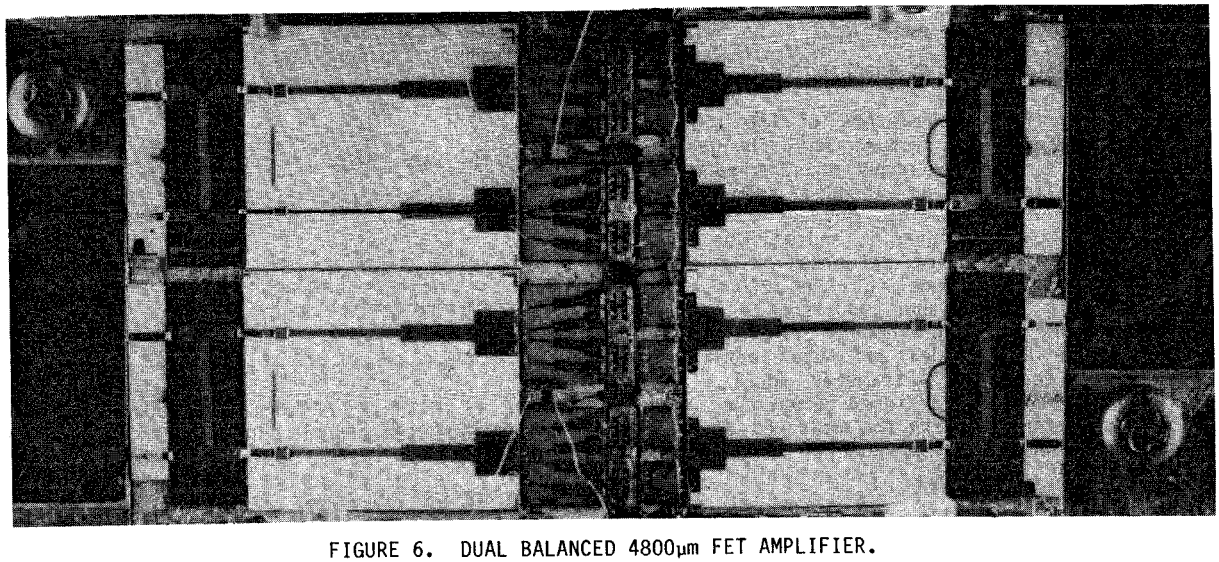

FIGURE 6. DUAL BALANCED 4800μm FET AMPLIFIER.

CIRCUIT FABRICATION

Developments in high dielectric low-loss ceramics have made materials available which can be used to fabricate very small low impedance networks. A .152mm thick substrate of dielectric constant 64 was chosen to realize the input and output networks for the 4800μm FET. Figure 4 compares the impedance and line width of .254mm thick alumina (K_r=9.9), and the .152mm thick high dielectric ceramic (K_r=64). The much smaller line widths are now comparable to the small size of the 1200μm cell. The circuit dimensions were calculated from available microstrip transmission line analysis with careful consideration to include dispersion effects into the design.[5]

The circuit on the high dielectric material was fabricated by standard thin-film techniques used on other ceramic substrates. Since thin film techniques are used, the electrical lengths of the parallel networks are closely controlled and efficient power combining is easily maintained. The parallel networks are combined with a 3 section quaterwave transformer built on .254mm alumina and transformed to the desired 50Ω system. Combining losses of separate amplifiers were minimized and coupler fine line geometries were improved by fabricating couplers and power dividers on quartz substrate material.

AMPLIFIER DESCRIPTION AND PERFORMANCE

The amplifier chain is made up of three stages shown in Figure 5. The first stage is a balanced 2400μm FET amplifier, the second is a balanced 4800μm FET amplifier, and the last shown in Figure 6, is two balanced 4800μm FET amplifiers using quadrature couplers and paralleled with a Wilkinson hybrid. The Wilkinson hybrid is made up of five Chebycheff coupled sections with thin film resistors for isolation. Figure 7 shows the Wilkinson hybrid circuit layout.

Each amplifier is built on a molybdenum carrier plate and is mounted in an aluminum enclosure for good heat sinking capability. Because of the large power dissipated by the 4800μm FET, the four cells were divided into two which allowed for more reliable soldering joints to the carrier plate. Drain bias is applied to a shunt stub and gate bias is connected through small gold wire wound inductors. Each amplifier was assembled, tested, placed into the fixture, and connected with gold ribbon.

Since the large-signal match resulted in a gain rolloff, a balanced equalizer was designed to be incorporated with the amplifier. Figure 8a shows the small-signal gain with the equalizer. The large-signal performance of the amplifier cascade at 1 dB compression is shown in Figure 8b. Four watt output was achieved over most of the band with an efficiency of 11.5 percent. Using the high dielectric networks, each amplifier was very repeatable, with bond wire lengths from the FET to matching networks being the major source of combining and matching losses.

CONCLUSION

Newly developed GaAs power FETs have larger gate widths and higher input Qs, which limit the effectiveness of conventional matching techniques. Because of developments in high dielectric ceramics, accurate high dielectric networks can be designed and fabricated to achieve wide-band, high power matching networks for GaAs FET amplifiers. Since transmission line theory for microstrip and thin film techniques has already been well established, the high dielectric networks are well suited for use in high-power, wideband GaAs FET amplifier applications.

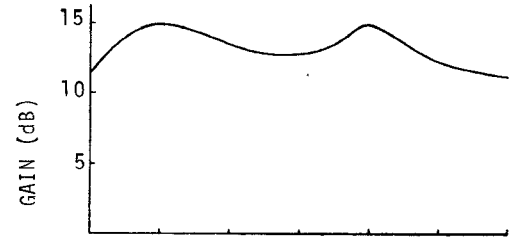

FIGURE 8a. SMALL SIGNAL GAIN OF AMPLIFIER CASCADE.

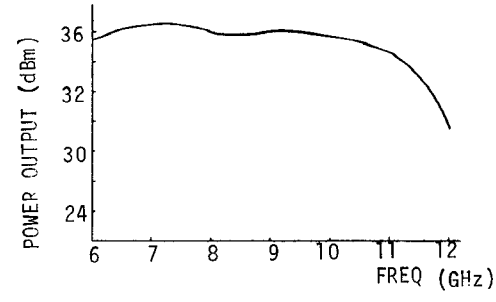

FIGURE 8b. OUTPUT POWER OF AMPLIFIER CASCADE AT 1dB COMPRESSION.

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